

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

023925-00015

SERIAL NO.

New Application

## LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

APPLICANT

TZENG

FILING DATE

August 31, 2001

GROUP

Not yet assigned

09/942789  
08/31/01

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
PD	AA	5,555,398	Sep. 10, 1996	Raman			Apr. 15, 1994
PD	AB	5,644,784	Jul. 1, 1997	Peek			Mar. 3, 1995
PD	AD	5,828,653	Oct. 27, 1998	Goss			Apr. 26, 1996
PD	AE	5,423,015	Jun. 6, 1995	Chung			May 21, 1991
PD	AF	5,696,899	Dec. 9, 1997	Kalwitz			Nov. 18, 1992
PD	AG	6,061,351	May 9, 2000	Erimil et al.			Dec. 18, 1997
PD	AH	5,748,631	May 5, 1998	Bergantino et al.			May 9, 1996
PD	AI	6,119,196	Sep. 12, 2000	Muller et al.			Jun. 30, 1997
PD	AJ	6,175,902 B1	Jan. 16, 2001	Runaldue et al.			Dec. 18, 1997
PD	AK	5,473,607	Dec. 5, 1995	Hausman et al.			Aug. 9, 1993
PD	AL	5,787,084	Jul. 28, 1998	Hoang et al.			Jun. 5, 1996
PD	AM	5,845,081	Dec. 1, 1998	Rangarajan et al.			Sep. 3, 1996
PD	AN	5,892,922	Apr. 6, 1999	Lorenz			Feb. 28, 1997
PD	AO	5,802,287	Sep. 1, 1998	Rostoker et al.			Aug. 3, 1995
PD	AP	6,011,795	Jan. 4, 2000	Varghese et al.			Mar. 20, 1997
PD	AQ	6,185,185 B1	Feb. 6, 2001	Bass et al.			Nov. 21, 1997
PD	AR	5,524,254	Jun. 4, 1996	Morgan et al.			Jul. 1, 1994
PD	AS	5,987,507	Nov. 16, 1999	Creedon et al.			Dec. 29, 1998
PD	AT	5,831,980	Nov. 3, 1998	Varma et al.			Sep. 13, 1996
PD	AU	5,781,549	Jul. 14, 1998	Dai			Feb. 23, 1996
PD	AV	6,041,053	Mar. 21, 2000	Douceur et al.			Sep. 18, 1997
PD	AW	5,459,717	Oct. 17, 1995	Mullan et al.			Mar. 25, 1994
PD	AX	5,909,686	Jun. 1, 1999	Muller et al.			Jun. 30, 1997
PD	AY	5,887,187	Mar. 23, 1999	Rostoker et al.			Apr. 14, 1997
PD	AZ	5,568,477	Oct. 22, 1996	Galand et al.			Jun. 27, 1995
PD	BA	5,414,704	May 9, 1995	Spinney			Apr. 5, 1994
PD	BB	5,390,173	Feb. 14, 1995	Spinney et al.			Oct. 22, 1992
PD	BC	5,825,772	Oct. 20, 1998	Dobbins et al.			Apr. 2, 1996
PD	BD	5,790,539	Aug. 4, 1998	Chao et al.			Jan. 29, 1996

# U.S. PATENT DOCUMENTS

Sheet 2 of 3

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
PA	BE	5,918,074	Jun 29, 1999	Wright et al.			Jul. 25, 1997
PA	BF	5,898,687	Apr. 27, 1999	Harriman et al.			Jul. 24, 1996
PA	BG	5,940,596	Aug. 17, 1999	Rajan et al.			Aug. 4, 1997
PA	BH	5,802,052	Sep. 1, 1998	Venkataraman			Jun. 26, 1996
PA	BI	5,842,038	Nov. 24, 1998	Williams et al.			Oct. 10, 1996
PA	BJ	5,742,613	Apr. 21, 1998	MacDonald			Apr. 27, 1993
PA	BK	5,579,301	Nov. 26, 1996	Ganson et al.			Feb. 28, 1994
PA	BL	5,278,789	Jan. 11, 1994	Inoue et al.			Dec. 6, 1991
PA	BM	5,652,579	Jul. 29, 1997	Yamada et al.			Aug. 15, 1996
PA	BN	5,499,295	Mar. 12, 1996	Cooper			Aug. 31, 1993

# FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION		
							YES	NO	PART.
PA	BO	WO/9900936	Jan. 7, 1999	WIPO			xx		
PA	BP	EP 0 465 090 A1	Jan. 8, 1992	EPO			xx		
PA	BQ	EP 0 859 492 A2	Aug. 19, 1998	EPO			xx		
PA	BR	EP 0 312 917 A2	Apr. 26, 1989	EPO			xx		
PA	BS	EP 0 853 441 A2	Jul. 15, 1998	EPO			xx		
PA	BT	4-189023	Jul. 7, 1992	Japan					Abs
PA	BU	WO 98/09473	Mar. 5, 1998	WIPO			xx		
PA	BV	EP 0 752 796 A2	Jan. 8, 1997	EPO			xx		
PA	BW	EP 0 862 349 A2	Sep. 2, 1998	EPO					Abs
PA	BX	FR 2 725 573	Apr. 12, 1996	France					Abs
PA	BY	EP 0 854 606 A2	Jul. 22, 1998	EPO			xx		
PA	BZ	WO 99/00948	Jan. 7, 1999	WIPO			xx		
PA	CA	WO 99/00949	Jan. 7, 1999	WIPO			xx		
PA	CB	WO 99/00950	Jan. 7, 1999	WIPO			xx		
PA	CC	WO 99/00939	Jan. 7, 1999	WIPO			xx		
PA	CD	WO 99/00938	Jan. 7, 1999	WIPO			xx		
PA	CE	WO 99/00944	Jan. 7, 1999	WIPO			xx		
PA	CF	WO 99/00945	Jan. 7, 1999	WIPO			xx		
PA	CG	EP 0 849 917 A2	Jun. 24, 1998	EPO			xx		
PA	CH	EP 0 907 300 A2	Apr. 7, 1999	EPO			xx		

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

Sheet 3 of 3

PJ	CI	"A High-Speed CMOS Circuit for 1.2-Gb/s 16 x 16 ATM Switching," Alain Chemarin et al. 8107 IEEE Journal of Solid-State Circuits 27(1992) July, No. 7, New York, US, pages 1116-1120
PJ	CJ	"Local Area Network Switch Frame Lookup Technique for Increased Speed and Flexibility," 700 IBM Technical Disclosure Bulletin 38(1995) July, No. 7, Armonk, NY, US, pages 221-222
PJ	CK	"Queue Management for Shared Buffer and Shared Multi-buffer ATM Switches," Yu-Sheng Lin et al., Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C., March 24, 1996, pages 688-695
PJ	CL	"A 622-Mb/s 8 x 8 ATM Switch Chip Set with Shared Multibuffer Architecture," Harufusa Kondoh et al., 8107 IEEE Journal of Solid-State Circuits 28(1993) July, No. 7, New York, US, pages 808-814
PJ	CM	"Catalyst 8500 CSR Architecture," White Paper XP-002151999, Cisco Systems Inc. 1998, pages 1-19
PJ	CN	"Computer Networks," A.S. Tanenbaum, PRENTICE-HALL INT., USA, XP-002147300(1998), Sec. 5.2-Sec. 5.3, pages 309-320

EXAMINER <i>Renell Jones</i>	DATE CONSIDERED <i>6/24/05</i>
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>	

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 58269.00015	SERIAL NO. 09/942,769
LIST OF REFERENCES CITED BY APPLICANT  (Use several sheets if necessary)		APPLICANT TZENG	
		FILING DATE August 31, 2001	GROUP 2661

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

RECEIVED

APR 26 2004

Technology Center 2600

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO PART.		
	AG	WO 00/03256	January 20, 2000	WIPO			XX		
	AH								
	AI								
	AJ								
	AK								

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	AL	Doganata, et al., "Effects of Cascading on the Performance of a Switching Subsystem," Proceedings of the Global Telecommunications Conference (Globecom), vol. 1, December 6, 1992, pages 1493-1497, XP010062487.
	AM	Level One: "Level One™ IXP1200 Network Processor", Level One, September 1999, XP002187948, URL: <a href="http://www.cs.utah.edu/cs6935/Previous/s01/netprocs/ixa/ixp1200ad.pdf">http://www.cs.utah.edu/cs6935/Previous/s01/netprocs/ixa/ixp1200ad.pdf</a> , page 26, January 22, 2002.
	AN	Noureddine, et al., "Selective Back-Pressure in Switched Ethernet Lans", 1999 IEEE Global Telecommunications Conference, vol. 2, December 5, 1999, pages 1256-1263, XP002258500.

EXAMINER <i>Phrell Jones</i>	DATE CONSIDERED <i>6/23/05</i>
---------------------------------	-----------------------------------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.